EXHIBIT U

Exhibit 13 – Xilinx Virtex-4 FPGA

'156 Patent

Claim Limitation (Claim 7)	Exemplary Disclosure
[**156a**] A device comprising:	The Xilinx Virtex-4 family of FPGAs ("Xilinx Virtex-4") discloses a device.[1] *See, e.g.*: "[T]he Virtex®-4 family from Xilinx greatly enhances programmable logic design capabilities, making it a powerful alternative to ASIC technology. Virtex-4 FPGAs comprise three platform families—LX, FX, and SX—offering multiple feature choices and combinations to address all complex applications. The wide array of Virtex-4 FPGA hard-IP core blocks includes the PowerPC® processors (with a new APU interface), tri-mode Ethernet MACs, 622 Mb/s to 6.5 Gb/s serial transceivers, dedicated DSP slices, high-speed clock management circuitry, and source-synchronous interface blocks." Virtex-4 Family Overview (Aug. 30, 2010), *available at* https://www.xilinx.com/support/documentation/data_sheets/ds112.pdf (hereinafter "Virtex-4 Family Overview").[2] "The DSP48 slice is a new element in the Xilinx development model referred to as Application Specific Modular Blocks (ASMBL™) architecture. The purpose of this model is to deliver off-the-shelf programmable devices with the best mix of logic, memory, I/O, processors, clock management, and digital signal processing." XtremeDSP for Virtex-4 FPGAs at 11 (May 15, 2008) (hereinafter "XtremeDSP"). "Each XtremeDSP tile contains two DSP48 slices to form the basis of a versatile coarse-grain DSP architecture. Many DSP designs follow a multiply with addition. In Virtex®-4 devices, these elements are

[1] The devices discussed in this chart are exemplary of Xilinx devices existing at the time of the alleged invention(s). Google is in the process of pursuing documents from Xilinx, a third party in this action, and Google reserves the right to amend its invalidity charts pending the results of its investigation and Xilinx's production. Thus, this chart should be treated as exemplary of other Xilinx devices and/or floating-point operator version(s) that may also meet the elements of the asserted claim in a manner similar to the charted materials. Indeed, public information suggests that the Virtex-5 and Virtex-6 were released prior to the date of the provisional application to which the patents-in-suit claim priority, and the Virtex-7 was released prior to the date of the earliest parent application to which the patents in suit claim priority. Furthermore, public information suggests that one or more versions of the Xilinx Floating Point operator, beyond the ones referenced herein, were released prior to the date of the provisional and/or earliest parent applications. Google is continuing to pursue discovery regarding these devices/systems.

[2] All Virtex-4 devices were released for production in 2007. *See* Virtex-4 Family Overview at 9.

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Claim Limitation (Claim 7)	Exemplary Disclosure
	supported in dedicated circuits." *Id.* "The DSP48 slices available in all Virtex-4 family members support new DSP algorithms and higher levels of DSP integration than previously available in FPGAs. Minimal use of general FPGA fabric leads to low power, very high performance, and efficient silicon utilization." *Id.*
[**156b**] at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	The Xilinx Floating-Point Operator, which is compatible with Xilinx Virtex-4 and DSP48, discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See, e.g.*: "The Xilinx Floating-Point core provides designers with the means to perform floating-point arithmetic on FPGA. The core can be customized to allow optimization for operation, word length, latency, and interface." XILINX-GOOG-SUB00000140. The Xilinx Floating-Point core is available for FPGAs including the Virtex-4, and "supports operators including multiply, add/subtract, divide, square-root, comparison, conversion from floating-point to fixed-point, conversion from fixed-point to floating point, conversion between floating-point types." XILINX-GOOG-SUB00000140. "The DSP48 slices support many independent functions, including multiplier, multiplier-accumulator (MACC), multiplier followed by an adder, three-input adder, barrel shifter, wide bus multiplexers, magnitude comparator, or wide counter. The architecture also supports connecting multiple DSP48 slices to form wide math functions, DSP filters, and complex arithmetic without the use of general FPGA fabric." Xtreme DSP at 11. "The Xilinx Floating-Point core allows a range of floating-point arithmetic operations to be performed on FPGAs. The operation is specified when the core is generated, and each variant has a common interface. This interface is shown in Figure 1. When a user selects an operation that requires only one operand, the B input is omitted." XILINX-GOOG-SUB00000140; Xilinx Floating-Point Operator v3.0 (Sept. 28, 2006) at 1 (hereinafter "Xilinx Floating-Point Operator v3.0").

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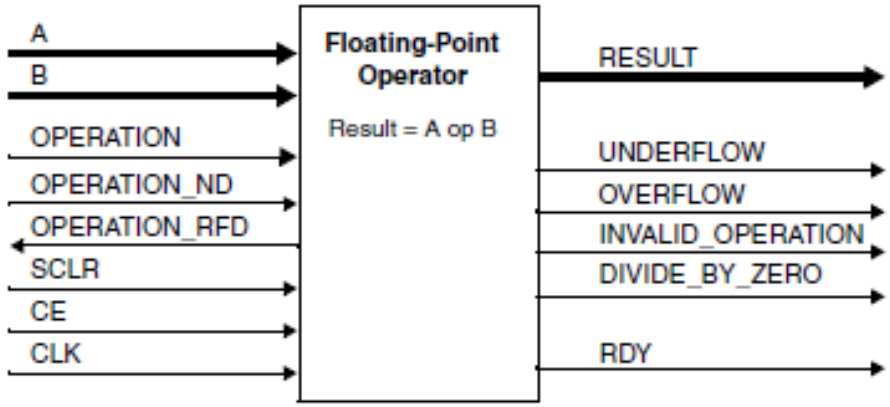
Claim Limitation (Claim 7)	Exemplary Disclosure
	 *Figure 1:* **Block Diagram of Generic Floating-Point Binary Operator Core** *Id.*

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Claim Limitation (Claim 7)	Exemplary Disclosure

Port Description

The ports employed by the core are shown in Figure 1. They are described in more detail in Table 2. All control signals are active high.

Table 2: **Core Ports**

Name	Width	Direction	Description
A[1]	w	INPUT	**Operand A**
B[1]	w	INPUT	**Operand B:** Only present on binary operation.
OPERATION[1]	6	INPUT	**Operation:** Specifies the operation to be performed. Implemented when the core is configured for both add and subtract operations, or as a programmable comparator.
OPERATION_ND	1	INPUT	**New Data:** Must be set high to indicate that operand A, operand B and OPERATION, when required, are valid.
OPERATION_RFD	1	OUTPUT	**Ready For Data:** Set high by core to indicate that it is ready for new operands.
SCLR	1	INPUT	**Synchronous Reset** (optional).
CE	1	INPUT	**Clock Enable** (optional).
CLK	1	INPUT	**Clock**
RESULT	w	OUTPUT	**Result Output:** Result of operation.
UNDERFLOW	1	OUTPUT	**Underflow:** Set high by core when underflow occurs. Supplied in synchronism with associated RESULT.
OVERFLOW	1	OUTPUT	**Overflow:** Set high by core when overflow occurs. Supplied in synchronism with associated RESULT.

XI LI NX-GOOG-SUB00000143; Xilinx Floating-Point Operator v3.0 at 5.

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Claim Limitation (Claim 7)	Exemplary Disclosure
	Optimization Selection This parameter allows the type of optimization to be selected. Note that the optimization selected will determine the additional core configuration information requested by subsequent GUI screens. The optimizations supported are: **Basic (unoptimized):** The cores offer a good balance between latency and clock rate. Basic core configurations include add, multiply, divide and compare operation types. The multiplier is only available on FPGA families that support embedded multipliers. (Note that multipliers are available for all families when the core is speed optimized). Only single formats are supported. For add/subtract, multiply and compare operations an operand can be issued on every clock cycle. However, to reduce resource requirements the divide operations is multi-cycle and only performs an operation every 30 cycles. **Speed Optimized:** The core is optimized for maximum throughput. Operands can be issued on every clock cycle and a high-level of pipelining is employed to maximize clock rate. The speed optimized core configurations include add, multiply, divide and square-root (sqrt) operation types. A range of operand widths is provided. The latency of the speed optimized core depends upon: - width of the operands - operator type - multiplier type (embedded or logic-based) used for multiply operation See "The latency of the basic add/subtract and multiply operations is 5 cycles. The latency of the compare operation is 2 cycles and the divide operation 30 cycles." on page 10 for specific values of latency. **Operation Type** The floating-point operation may be one of the following: • **Add** **Subtract** **Multiply** **Divide** **Square-root** (only available with speed optimization) **Compare** (not available with speed optimization). XILINX-GOOG-SUB00000147.

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<table>
<tr><th>Claim Limitation (Claim 7)</th><th>Exemplary Disclosure</th></tr>
<tr><td></td><td>
Width of the Operand and Results
The format widths supported for speed optimized cores is summarized in Table 5. For each valid wordlength configuration, the total format width is also shown in Table 5.
Table 5: Supported Widths for Speed Optimized Cores
<table>
<tr><th rowspan="3">Fraction Width</th><th colspan="5">Width</th></tr>
<tr><th colspan="5">Exponent Width</th></tr>
<tr><th>4</th><th>6</th><th>8</th><th>10</th><th>11</th></tr>
<tr><td>8</td><td>12</td><td>14</td><td></td><td></td><td></td></tr>
<tr><td>10</td><td>14</td><td>16</td><td></td><td></td><td></td></tr>
<tr><td>12</td><td>16</td><td>18</td><td></td><td></td><td></td></tr>
<tr><td>14</td><td></td><td>20</td><td>22</td><td></td><td></td></tr>
<tr><td>16</td><td></td><td>22</td><td>24</td><td></td><td></td></tr>
<tr><td>17</td><td></td><td>23</td><td>25</td><td></td><td></td></tr>
<tr><td>20</td><td></td><td>26</td><td>28</td><td>30</td><td></td></tr>
</table>
XILINX-GOOG-SUB00000148.
</td></tr>
<tr><td>[156c] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at</td><td>The Xilinx Floating Point Operator discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. Specifically, the Xilinx Floating Point Operator supports an 8-bit fraction and a 6-bit exponent, which meets the claimed minimum error rate. See e.g.:</td></tr>
</table>

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Claim Limitation (Claim 7)	Exemplary Disclosure
least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and	**Width of the Operand and Results** The format widths supported for speed optimized cores is summarized in Table 5. For each valid wordlength configuration, the total format width is also shown in Table 5. Table 5: **Supported Widths for Speed Optimized Cores** **Fraction Width** / **Width** / **Exponent Width** 4 | 6 | 8 | 10 | 11 8 | 12 | 14 | | | | 10 | 14 | 16 | | | | 12 | 16 | 18 | | | | 14 | | 20 | 22 | | | 16 | | 22 | 24 | | | 17 | | 23 | 25 | | | 20 | | 26 | 28 | 30 | | XILINX-GOOG-SUB00000148.

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Claim Limitation (Claim 7)	Exemplary Disclosure

The latency of the speed optimized Floating-Point core is tabulated for all supported width and operation types in Table 6.

Table 6: **Latency of Speed Optimized Core**

Core Parameters		Latency (cycles)					
Fraction width	Exponent width	Add	Multiply				Divide and Sqrt
			Logic only	MULT18X18	DSP48	DSP48 + logic	
8	4 & 6	10	6	5	6	6	11
10	4 & 6	10	6	5	6	6	12
12	4 & 6	10	7	5	6	6	15
14	6 & 8	10	7	5	6	6	17
17	6 & 8	11	7	5	6	6	20
20	6, 8 & 10	11	7	6	9	11	23
22	6, 8 & 10	11	7	6	9	11	25
24	6, 8, & 10	11	8	6	9	11	27
34	8	12	8	6	9	9	37
53	11	12	9	10	21	17	56

XIXLINX-GOOG-SUB0000149.

The Xilinx Floating-Point core is available for FPGAs including the Virtex-4, and supports operators including multiply, add/subtract, divide, square-root, comparison, "conversion from floating-point to fixed-point," "conversion from fixed-point to floating point," and "conversion between floating-point types." Floating-Point Operator 3.0 at 1.

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Claim Limitation (Claim 7)	Exemplary Disclosure
	"The maximum latency of the divide and square root operations is fraction width + 4, and for compare operation it is three cycles. The float-to-float conversion operation is three cycles when either mantissa or exponent width is being reduced, otherwise it is two cycles." *Id.* at 13. To the extent that Singular contends that the Xilinx Floating Point Operator and the Xilinx Virtex-4 SX do not disclose this limitation, notwithstanding their disclosure of a floating point format with 8 fraction bits and 6 exponent bits, that format would have been obvious to one of skill in the art for the reasons explained in the Responsive Contentions Regarding Non-Infringement and Invalidity ("Responsive Contentions"). Among other things, the Responsive Contentions explain how those skilled in the art would mix and match formats depending on application specific needs. Specifically, the Responsive Contentions explain that the reduced-precision formats disclosed in any of Dockser, Lee, Belanović, Belanović and Leeser, Sudha, Shirazi, Aty, and TMS320C32 would have motivated one of skill in the art to implement them in an FPGA, and/or to implement the 8-bit fraction and 6-bit exponent format of the Xilinx Floating-Point core. As one example, based on the disclosure of the Belanović thesis, one of skill in the art would have understood the different combinations of fraction and exponent bits (*e.g.*, 5 fraction bits, 6 exponent bits, and one sign bit, for a total of 12 bits) would have been possible and even desired depending on the application. Indeed, one of skill in the art would have been motivated to apply the teachings of Tong, which disclosed a 5-bit mantissa and 6-bit exponent (*see* Tong chart), to which Belanović cites. *See* Belanović, *Library of Parameterized Hardware* at 73, n.21. *See also* Appendix to Responsive Contentions (detailing error rates associated with different mantissa sizes).
[**156d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit;	The Xilinx Virtex-4 teaches or suggests at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See, e.g.*: "[T]he Virtex®-4 family from Xilinx greatly enhances programmable logic design capabilities, making it a powerful alternative to ASIC technology. Virtex-4 FPGAs comprise three platform families—LX, FX, and SX—offering multiple feature choices and combinations to address all complex applications. The wide array of Virtex-4 FPGA hard-IP core blocks includes the PowerPC® processors (with a new APU interface), tri-mode Ethernet MACs, 622 Mb/s to 6.5 Gb/s serial transceivers, dedicated DSP slices, high-speed clock management circuitry, and source-synchronous interface blocks." Virtex-4 Family Overview at 1. "The Xilinx Floating-Point core provides designers with the means to perform floating-point arithmetic on

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Claim Limitation (Claim 7)	Exemplary Disclosure
	FPGA. The core can be customized to allow optimization for operation, word length, latency, and interface." XILINX-GOOG-SUB00000140. To the extent that Singular contends that the Xilinx Floating Point Operator and the Xilinx Virtex-4 SX do not disclose this limitation, notwithstanding their disclosure of an FPGA running a floating-point operator, this limitation would have been obvious to one of skill in the art for the reasons explained in the Responsive Contentions. In particular, it would have been obvious to combine a Xilinx FPGA operating Xilinx Floating Point Core software with a controller board like Wildstar. As reflected in Pavle Belanović's thesis, *Library of Parameterized Hardware Modules for Floating-Point Arithmetic with an Example Application*, and his related article with Miriam Leeser, *Library of Parameterized Floating-Point Modules and Their Use*, many reconfigurable computing systems are based on one or more FPGAs connected to a number of memory banks. All designs presented by Belanović and Leeser are implemented on the Wildstar reconfigurable computing engine from Annapolis Micro Systems. Figure 1.2 shows the structure of this board.

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Claim Limitation (Claim 7)	Exemplary Disclosure

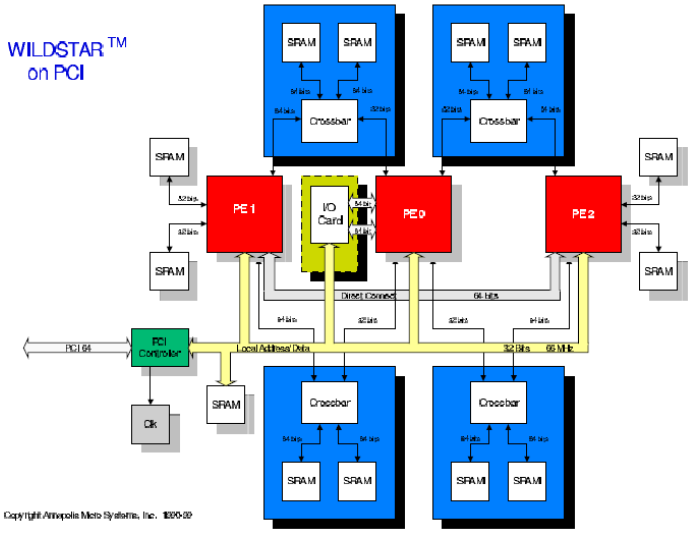

Figure 1.2: Structure of the Wildstar reconfigurable computing engine

Some of the main features of the Wildstar board are:

- 3 Xilinx VIRTEX XCV1000 FPGAs,
- total of 3 million system gates,
- 40 Mbytes of SRAM,
- 1.6 Gbytes/sec I/O bandwidth,
- 6.4 Gbytes/sec memory bandwidth,
- processing clock rates up to 100MHz."

Belanović, *Library of Parameterized Hardware* at 14.

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Claim Limitation (Claim 7)	Exemplary Disclosure
[**156e**] wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine;	Xilinx Virtex-4 teaches or suggests at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine. Specifically, Xilinx Virtex-4 SX discloses an FPGA. *See, e.g.*: "[T]he Virtex®-4 family from Xilinx greatly enhances programmable logic design capabilities, making it a powerful alternative to ASIC technology. Virtex-4 FPGAs comprise three platform families—LX, FX, and SX—offering multiple feature choices and combinations to address all complex applications. The wide array of Virtex-4 FPGA hard-IP core blocks includes the PowerPC® processors (with a new APU interface), tri-mode Ethernet MACs, 622 Mb/s to 6.5 Gb/s serial transceivers, dedicated DSP slices, high-speed clock management circuitry, and source-synchronous interface blocks." Virtex-4 Family Overview at 1. To the extent that Singular contends that Xilinx Virtex-4 SX does not disclose this limitation, notwithstanding its disclosure of an FPGA, this limitation would have been obvious to one of skill in the art for the reasons explained in the Responsive Contentions. In particular, it would have been obvious to combine a Xilinx FPGA operating Xilinx Floating Point core software with a controller board like Wildstar. As reflected in Pavle Belanović's thesis, *Library of Parameterized Hardware Modules for Floating-Point Arithmetic with an Example Application*, and his related article with Miriam Leeser, *Library of Parameterized Floating-Point Modules and Their Use*, they made and used a system with at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine. Specifically, Belanović discloses a "host" computer that comprises at least a "state machine," "FPGAs," and various "processing units." *See, e.g.,* Belanović, *Library of Parameterized Hardware* at 15 (Fig 1.2) (depicting the Wildstar computer engine, including (1) a PCI 64, which implies an interconnection with a PC and thus a CPU, and (2) an I/O Card and Controller, which qualifies as a state machine). Some of the main features of the Wildstar board are: • 3 Xilinx VIRTEX XCV1000 FPGAs, • total of 3 million system gates, • 40 Mbytes of SRAM, • 1.6 Gbytes/sec I/O bandwidth,

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<table>
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<tr><td></td><td>• 6.4 Gbytes/sec memory bandwidth,
• processing clock rates up to 100MHz.”

Belanović, Library of Parameterized Hardware at 14.</td></tr>
<tr><td>[156f] and, wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</td><td>Xilinx Virtex-4 discloses the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. Specifically, the Xilinx Virtex-4 devices contain up to 512 DSP48 slices for each device. See, e.g.:

Number of DSP48 Slices Per Virtex-4 Device

Table 1-1 shows the number of DSP48 slices for each device in the Virtex-4 families. The Virtex-4 SX family offers the highest ratio of DSP48 slices to logic, making it ideal for math-intensive applications.

Table 1-1: Number of DSP48 Slices per Family Member
<table><tr><th>Device</th><th>DSP48</th><th>Columns</th><th>Device</th><th>DSP48</th><th>Columns</th><th>Device</th><th>DSP48</th><th>Columns</th></tr><tr><td>XC4VLX15</td><td>32</td><td>1</td><td>XC4VSX25</td><td>128</td><td>4</td><td>XC4VFX12</td><td>32</td><td>1</td></tr><tr><td>XC4VLX25</td><td>48</td><td>1</td><td>XC4VSX35</td><td>192</td><td>4</td><td>XC4VFX20</td><td>32</td><td>1</td></tr><tr><td>XC4VLX40</td><td>64</td><td>1</td><td>XC4VSX55</td><td>512</td><td>8</td><td>XC4VFX40</td><td>48</td><td>1</td></tr><tr><td>XC4VLX60</td><td>64</td><td>1</td><td></td><td></td><td></td><td>XC4VFX60</td><td>128</td><td>2</td></tr><tr><td>XC4VLX80</td><td>80</td><td>1</td><td></td><td></td><td></td><td>XC4VFX100</td><td>160</td><td>2</td></tr><tr><td>XC4VLX100</td><td>96</td><td>1</td><td></td><td></td><td></td><td>XC4VFX140</td><td>192</td><td>2</td></tr><tr><td>XC4VLX160</td><td>96</td><td>1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>XC4VLX200</td><td>96</td><td>1</td><td></td><td></td><td></td><td></td><td></td><td></td></tr></table></td></tr>
</table>

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Claim Limitation (Claim 7)	Exemplary Disclosure
	XtremeDSP at 13-14. The Xilinx Floating-Point Core features include "[s]upport for DSP48 on Virtex-4." XILINX-GOOG-SUB00000140; *see also* Floating-Point Operator v3.0 at 1 (includes "[s]upport for DSP48 on Virtex-4 FPGAs and DSP48E on Virtex-5 FPGAs"); Virtex-4 Family Overview at 1 (features include "ExtremeDSP Slice"). To the extent that Singular contends that Xilinx Virtex-4 does not identify a device with at least 100 multiplication execution units, notwithstanding its disclosure of a system with 512 such units, such a device would have been obvious for the reasons explained in the Responsive Contentions.

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'273 Patent

Claim Limitation (Claim 53)	Exemplary Disclosure
[**273a**] A device:	Xilinx Virtex-4 discloses a device. *See* [**156a**].
[**273b**] comprising at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	The Xilinx Floating-Point Operator, which is compatible with Xilinx Virtex-4 and the DSP48, discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**273c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;	The Xilinx Floating-Point Operator discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**]; *see also* Appendix to Responsive Contentions (detailing error rates associated with different mantissa sizes).

Exhibit 13 – Xilinx Virtex-4 FPGA

Claim Limitation (Claim 53)	Exemplary Disclosure
[**273d**] wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	Xilinx Virtex-4 discloses the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. *See* [**156f**].

'961 Patent

Claim Limitation (Claim 4)	Exemplary Disclosure
[**961a**] A device comprising:	Xilinx Virtex-4 discloses a device. *See* [**156a**].
[**961b**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Xilinx Virtex-4 discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**961c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to	Xilinx Virtex-4 discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**]; *see also* Appendix to Responsive Contentions (detailing error rates associated with different mantissa sizes).

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Claim Limitation (Claim 4)	Exemplary Disclosure
the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and	
[**961d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit.	Xilinx Virtex-4 SX, teaches or suggests at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See* [**156d**].

Claim Limitation (Claim 13)	Exemplary Disclosure
[**961e**] A device comprising:	Xilinx Virtex-4 SX, discloses an example device. *See* [**156a**].
[**961f**] a plurality of components comprising:	Xilinx Virtex-4 SX, discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* **[156b].** *See also* Xilinx Virtex-4 SX, discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See above* [**156d**].
[**961g**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	The Xilinx Floating Point Operator discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].

Exhibit 13 – Xilinx Virtex-4 FPGA

Claim Limitation (Claim 13)	Exemplary Disclosure
[**961h**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input.	The Xilinx Floating Point Operator discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**]; *see also* Appendix to Responsive Contentions (detailing error rates associated with different mantissa sizes).